Register No : _____

THE KAVERY ENGINEERING COLLEGE

(An Autonomous Institution)

B.E/B.TECH DEGREE END SEMESTER THEORY EXAMINATIONS, NOV /DEC 2024

Fourth Semester

Biomedical Engineering

BM3402 - Analog and Digital Integrated Circuits

Regulations - 2021

Duration : 3 Hrs *Maximum : 100 Marks*

*PART – A (ANSWER ALL QUESTIONS) (Marks 10*2=20)*

Q.No	*Questions*	*BLT*	*CO*	*Marks*
1.	Define CMRR in OP-AMP.	RE	1	2
2.	Illustrate integrator circuit.	UN	1	2
3.	Define sample and hold circuit.	RE	2	2
4.	List the various types of DAC and ADC.	RE	2	2
5.	Convert the given gray code (1011011101) into binary code.	AP	3	2
6.	Recall De Morgan's law.	RE	3	2
7.	Differentiate sum and carry.	UN	4	2
8.	What is magnitude comparator?	RE	4	2
9.	List out the various types of flip-flops.	RE	5	2
10.	Define universal shift register.	RE	5	2

*PART – B (ANSWER ALL QUESTIONS) (Marks 5*13 = 65)*

Q.No			*Questions*	*BLT*	*CO*	*Marks*
11.	a	i	Explain the non-inverting amplifiers using Op-Amp and Obtain the gain expressions.	UN	1	7
		ii	Illustrate the Differentiator schematic using Op-Amp.	UN	1	6
			Or			
	b	i	Explain in detail Astable multivibrator using Op - Amp with a neat diagram.	UN	1	7
		ii	Illustrate the instrumentation amplifier using Op-Amp.	UN	1	6
12.	a		Construct a binary weighted DAC. Solve the output voltage V_o forbinary combinations if R= 2.2K'Ω, R_f=1K'Ω and V_R=12V. (i) 1101, (ii) 01010, (iii) 110011	AP	2	13
			Or			
	b		Build the schematic diagram of VCO and explain it. Develop the Lock in range of PLL and capture range of PLL.	AP	2	13

13.	a		Model the 4 bit binary to gray code conversion and vice versa with implementation of circuit diagram using K-Map.	AP	3	13
			Or			
	b		Make use of K'Map in SOP & POS, simplify the following Boolean functions. F (w, x, y, z) = Σm (1, 3, 6, 9, 11, 12, 14).	AP	3	13
14.	a		Develop a 4 bit carry look ahead Adder using half adder and full adder circuit.	AP	4	13
			Or			
	b		Make use of logic gates develop 3 to 8 decoder with its truth table.	AP	4	13
15.	a		Design a 4-bit ripple counter with schematic diagram using K map.	AP	5	13
			Or			
	b		Design a 4-bit SISO and PIPO shift register sequential logic circuit with flip flops.	AP	5	13

*PART – C (Marks 1*15 = 15)*

Q.No			*Questions*	*BLT*	*CO*	*Marks*
16.	a	i	Construct 8-1 Multiplexer with necessary circuit diagram.	AP	4	10
		ii	Construct 1-4 demultiplexer with necessary circuit diagram.	AP	4	5
			Or			
	b	i	Make use of K-map technique and implementing gates, reduce the Boolean function f (w, x, y, z) = Σm (0,1,4,8,9,10) which has the don't cares condition d (w, x, y, z) = Σm (2,11).	AP	3	11
		ii	Solve $(4)_{10}$ - $(9)_{10}$ using the 2'S complement method.	AP	3	4